www.DataSheet4U.com

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistors
Logic Level TMOS (L²TMOS™)
D²PAK for Surface Mount

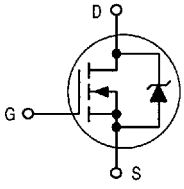
N–Channel Enhancement–Mode Silicon Gate

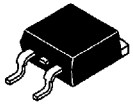
MTB30N06EL
Motorola Preferred Device

TMOS POWER FET
LOGIC LEVEL
30 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.05 OHM

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. The D²PAK contains an advanced TMOS E–FET die designed to withstand high energy in the avalanche mode and switch efficiently. This device is designed for use in low voltage, high speed switching applications such as power supplies, dc/dc converters, PWM motor controls or any application where the MOSFET will be operating into an inductive load.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number





CASE 418B–02, Style 2
D²PAK

7

DataSheet4U.com

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±15	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \leq 10$ µs)	I_D I_D I_{DM}	30 20 120	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted with the minimum recommended pad size	P_D	100 0.8 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vpk, I_L = 30 Apk, L = 0.49 mH, R_G = 25 Ω)	E_{AS}	220	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.25 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

DataSheet4U.com
www.DataSheet4U.com

REV 1

DataSheet4U.com

www.DataSheet4U.com

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 µAdc) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	60 —	— 62	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0) (V_{DS} = 60 Vdc, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— —	— —	0.25 1.0	mAdc
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 µAdc) Temperature Coefficient (Negative)	$V_{GS(th)}$	1.0 —	1.5 4.5	2.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 5.0 Vdc, I_D = 15 Adc) (V_{GS} = 4.0 Vdc, I_D = 15 Adc)	$R_{DS(on)}$	— —	0.03 0.04	0.05 0.07	Ohm
Drain–Source On–Voltage (V_{GS} = 5.0 Vdc) (I_D = 30 Adc) (I_D = 15 Adc, T_J = 125°C)	$V_{DS(on)}$	— —	— —	1.8 1.5	Vdc
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 15 Adc)	g_{FS}	13	—	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	—	1870	2600	pF
Output Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	530	800	
Reverse Transfer Capacitance	C_{rss}	—	50	100	
SWITCHING CHARACTERISTICS (2)					
Turn–On Delay Time	$t_{d(on)}$	—	12	25	ns
Rise Time (V_{DD} = 30 Vdc, I_D = 30 Adc, V_{GS} = 5.0 Vdc, R_G = 10 Ω)	t_r	—	156	300	
Turn–Off Delay Time	$t_{d(off)}$	—	36	70	
Fall Time	t_f	—	87	160	
Gate Charge	Q_T	—	22	40	nC
(V_{DS} = 48 Vdc, I_D = 30 Adc, V_{GS} = 5.0 Vdc)	Q_1	—	5.0	—	
	Q_2	—	10	—	
	Q_3	—	11	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage (I_S = 30 Adc, V_{GS} = 0) (I_S = 30 Adc, V_{GS} = 0, T_J = 125°C)	V_{SD}	— —	0.9 0.8	1.6 —	Vdc
Reverse Recovery Time (I_S = 30 Adc, V_{GS} = 0, dI_S/dt = 100 A/µs)	t_{rr}	—	48	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the tab to center of die)	L_D	—	3.5	—	nH
Internal Source Inductance (Measured from the source lead 0.1″ from package to source bond pad)	L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

DataSheet4U.com
www.DataSheet4U.com

www.DataSheet4U.com

TYPICAL ELECTRICAL CHARACTERISTICS

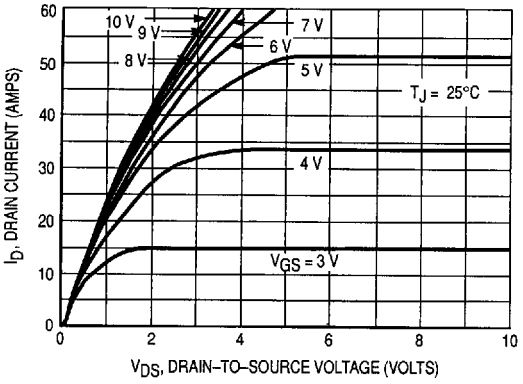


Figure 1. On–Region Characteristics

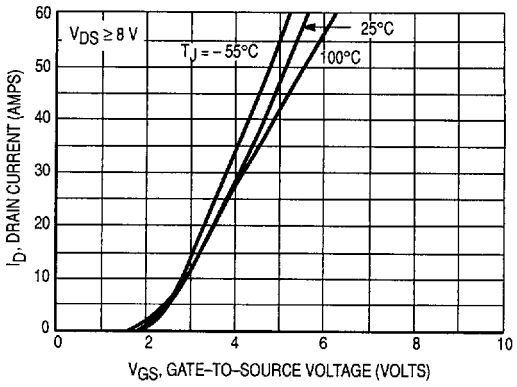


Figure 2. Transfer Characteristics

et4U.com

7

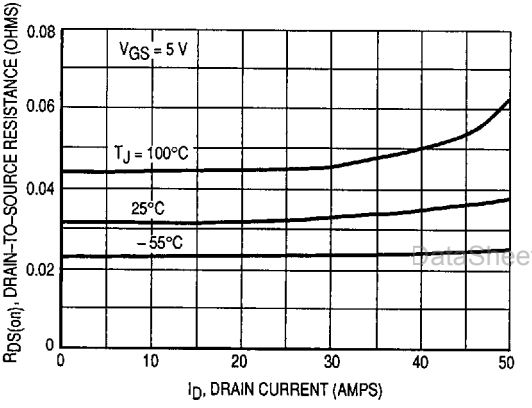


Figure 3. On–Resistance versus Drain Current

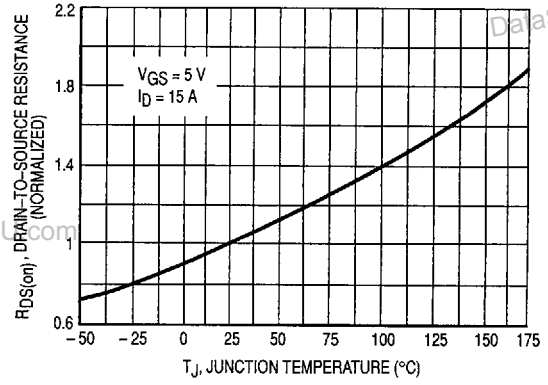


Figure 4. On–Resistance Variation With Temperature

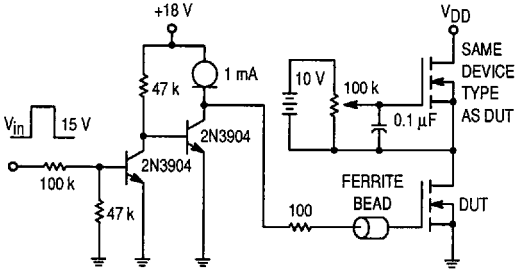


Figure 5. Gate Charge Test Circuit

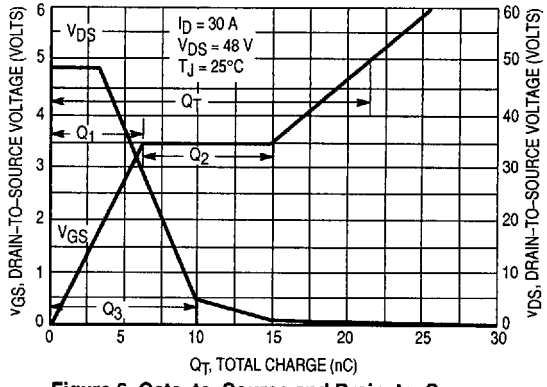


Figure 6. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 8) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

DataSheet4U.com www.DataSheet4U.com

www.DataSheet4U.com

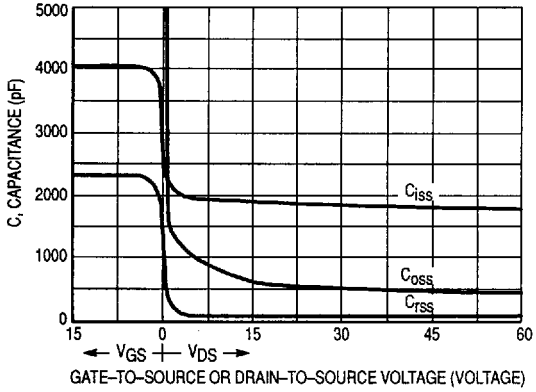


Figure 7. Capacitance Variation

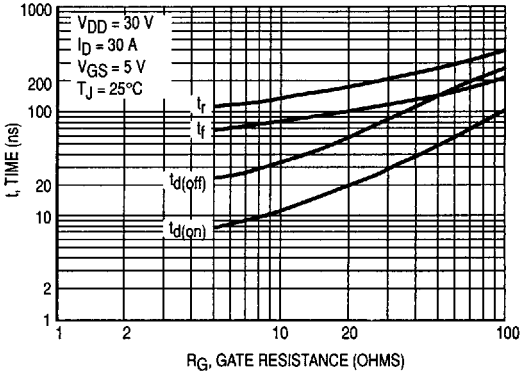


Figure 8. Resistive Switching Time Variation versus Gate Resistance

et4U.com

7

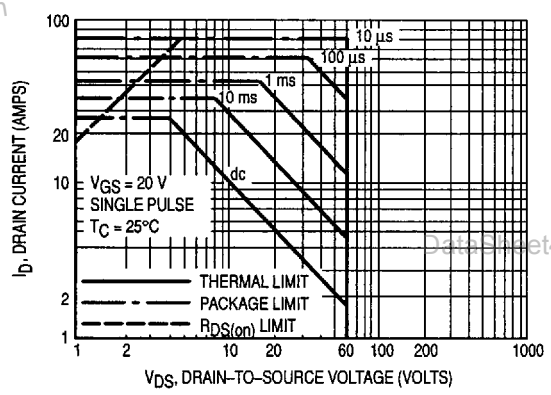


Figure 9. Maximum Rated Forward Biased Safe Operating Area

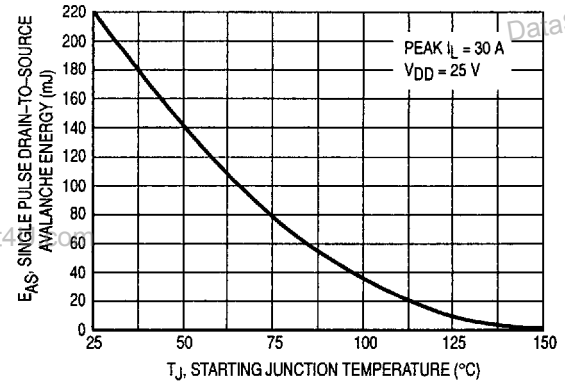


Figure 10. Maximum Avalanche Energy versus Starting Junction Temperature

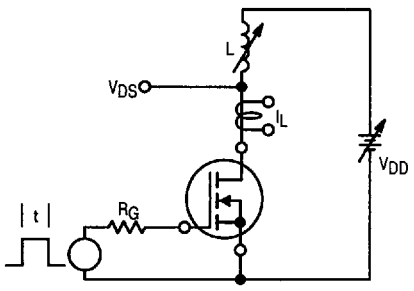


Figure 11. Unclamped Inductive Switching Test Circuit

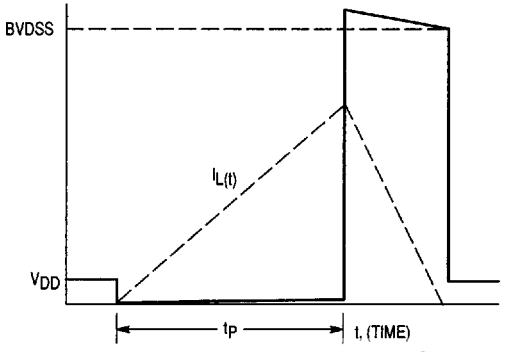


Figure 12. Unclamped Inductive Switching Waveforms

DataSheet4U.com
www.DataSheet4U.com

DataSheet4U.com

www.DataSheet4U.com

SAFE OPERATING AREA INFORMATION

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance–General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 11 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, BV_{DSS}. The switching SOA shown in Figure 11 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must not exceed $T_{J(max)} - T_C/R_{\theta JC}$.

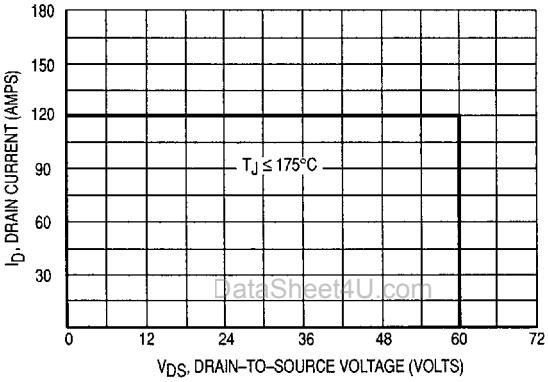


Figure 13. Maximum Rated Switching Safe Operating Area

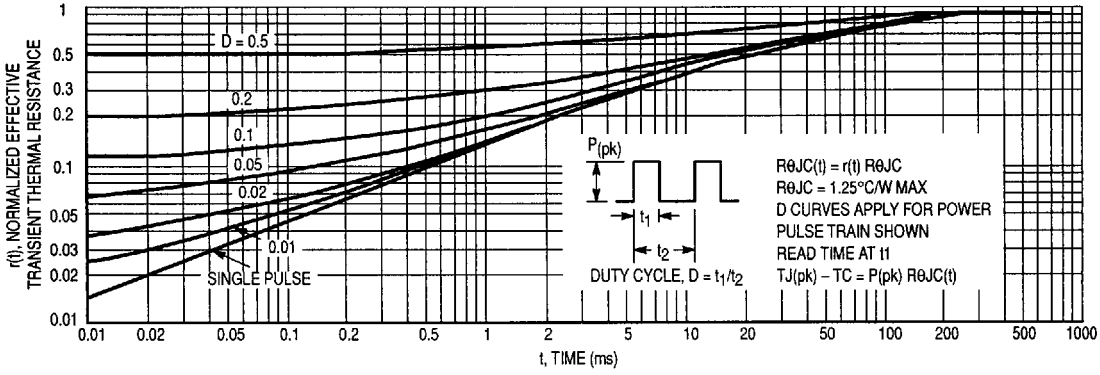


Figure 14. Thermal Response

DataSheet4U.com
www.DataSheet4U.com